FAIRCHILD SEMICONDUCTOR®

March 2008

# FDMS3662

## N-Channel Power Trench® MOSFET

### 100V, 49A, 14.8mΩ

### Features

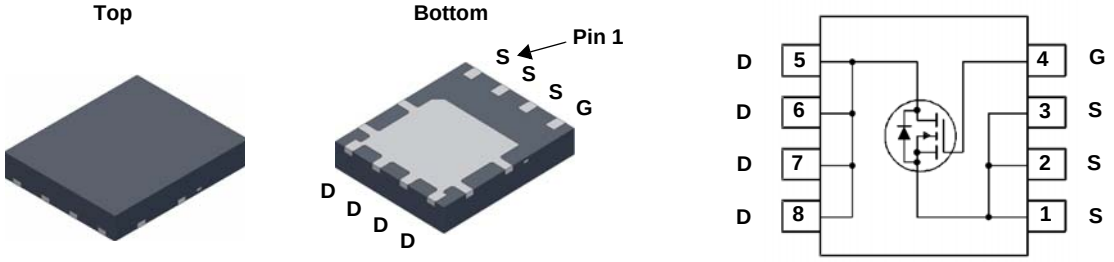
- Max $r_{DS(on)}$ = 14.8mΩ at $V_{GS}$ = 10V, $I_D$ = 8.9A
- Advanced Package and Silicon combination for low $r_{DS(on)}$
- MSL1 robust package design
- 100% UIL Tested
- RoHS Compliant

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- DC - DC Conversion




Power 56

## MOSFET Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 100 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±20 | V |
| $I_D$ | Drain Current -Continuous (Package limited) | $T_C$ = 25°C | | 49 | A |
| | -Continuous (Silicon limited) | $T_C$ = 25°C | | 57 | |
| | -Continuous | $T_A$ = 25°C | (Note 1a) | 8.9 | |
| | -Pulsed | | | 90 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | (Note 3) | 384 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25°C | | 104 | W |
| | Power Dissipation | $T_A$ = 25°C | (Note 1a) | 2.5 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to +150 | °C |

### Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 1.2 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 50 | |

### Package Marking and Ordering Information

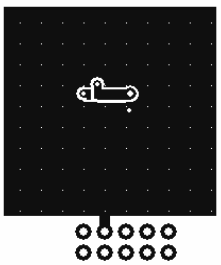
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMS3662 | FDMS3662 | Power 56 | 13" | 12mm | 3000 units |

## Electrical Characteristics $T_J$ = 25°C unless otherwise noted

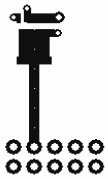
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250μA, $V_{GS}$ = 0V | 100 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250μA, referenced to 25°C | | 74 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{GS}$ = 0V, $V_{DS}$ = 80V, | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20V, $V_{DS}$ = 0V | | | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 2.5 | 3.5 | 4.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250μA, referenced to 25°C | | -10.8 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10V, $I_D$ = 8.9A | | 11.4 | 14.8 | mΩ |
| | | $V_{GS}$ = 10V, $I_D$ = 8.9A, $T_J$ = 125°C | | 19.0 | 24.7 | |
| $g_{FS}$ | Forward Transconductance | $V_{DD}$ = 10V, $I_D$ = 8.9A | | 37 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 50V, $V_{GS}$ = 0V, f = 1MHz | | 3470 | 4620 | pF |
| $C_{oss}$ | Output Capacitance | | | 245 | 325 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 110 | 165 | pF |
| $R_g$ | Gate Resistance | f = 1MHz | | 1.4 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 50V, $I_D$ = 8.9A, $V_{GS}$ = 10V, $R_{GEN}$ = 6Ω | | 25 | 40 | ns |
| $t_r$ | Rise Time | | | 15 | 26 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 32 | 52 | ns |
| $t_f$ | Fall Time | | | 6 | 10 | ns |
| $Q_g$ | Total Gate Charge at 10V | $V_{DD}$ = 50V, $I_D$ = 8.9A | | 54 | 75 | nC |
| $Q_{gs}$ | Gate to Source Charge | | | 18 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | 15 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0V, $I_S$ = 8.9A (Note 2) | | 0.8 | 1.3 | V |
| | | $V_{GS}$ = 0V, $I_S$ = 2.1A (Note 2) | | 0.7 | 1.2 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 8.9A, di/dt = 100A/μs | | 45 | 73 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 71 | 115 | nC |

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in$^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1 in$^2$ pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. Starting $T_J$ = 25°C, L = 3mH, $I_{AS}$ = 16A, $V_{DD}$ = 100V, $V_{GS}$ = 10V

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

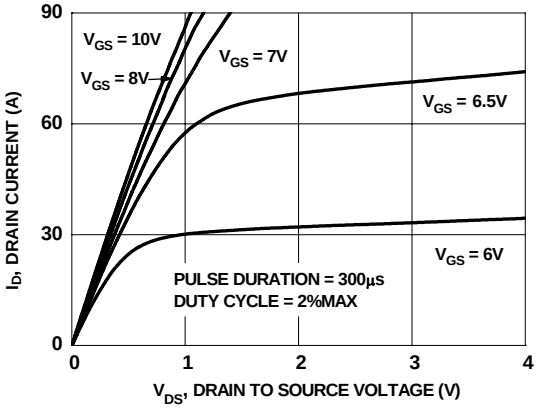



**Figure 1. On-Region Characteristics**

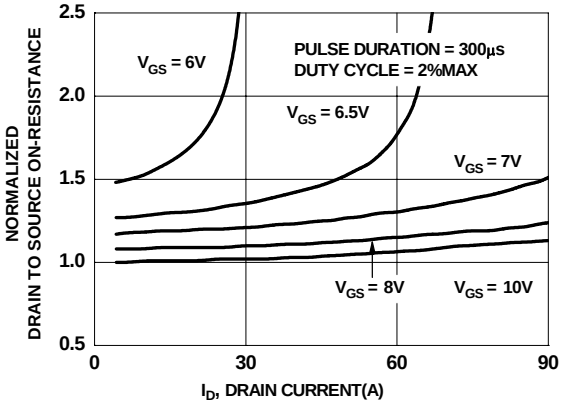



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

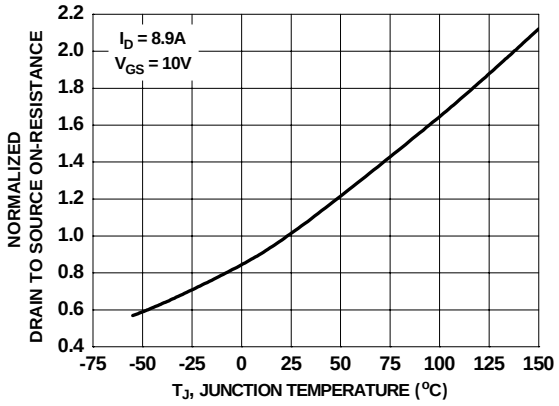



**Figure 3. Normalized On-Resistance vs Junction Temperature**

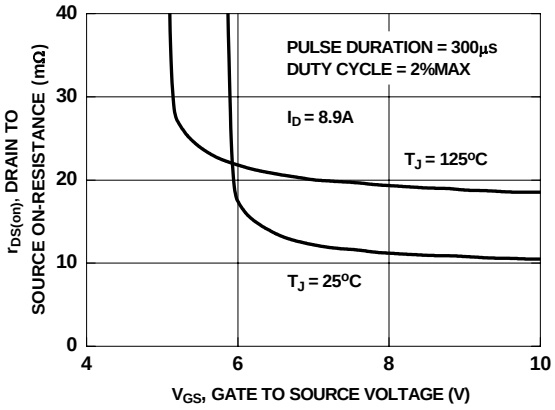



**Figure 4. On-Resistance vs Gate to Source Voltage**

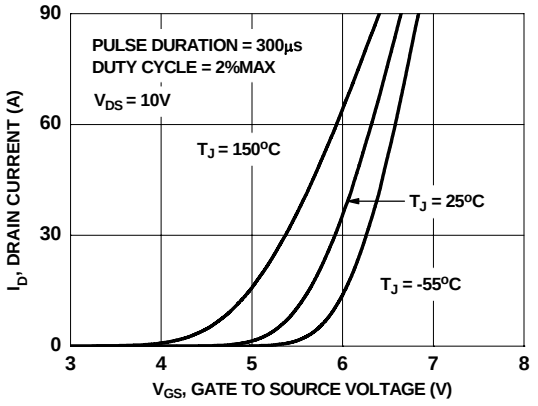



**Figure 5. Transfer Characteristics**

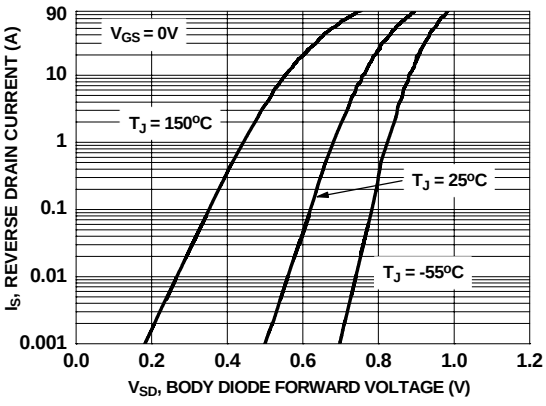



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

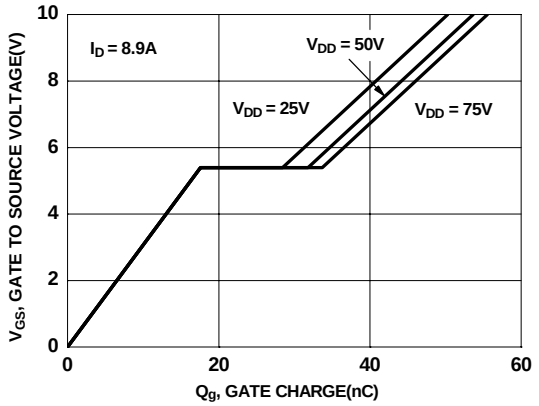



**Figure 7. Gate Charge Characteristics**

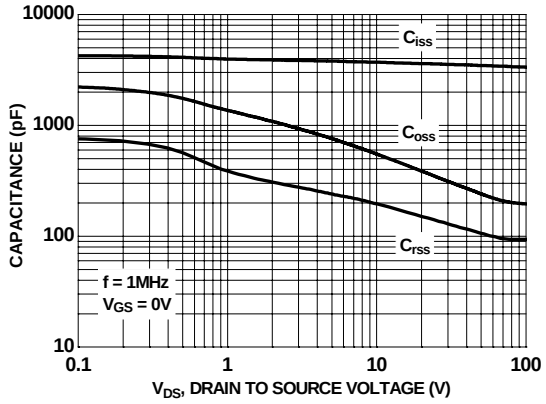



**Figure 8. Capacitance vs Drain to Source Voltage**

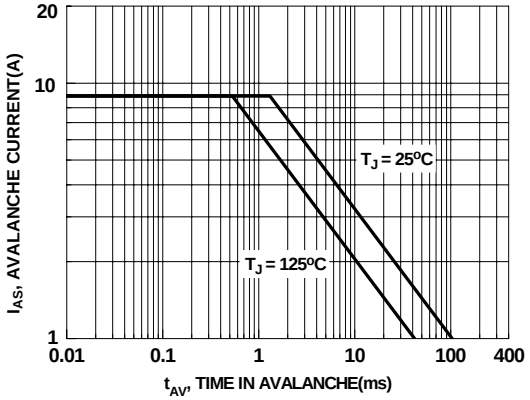



**Figure 9. Unclamped Inductive Switching Capability**

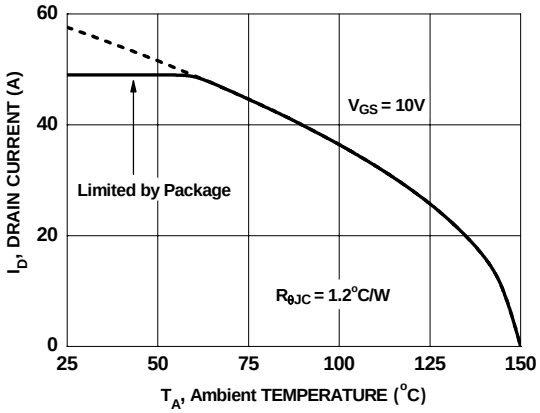



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

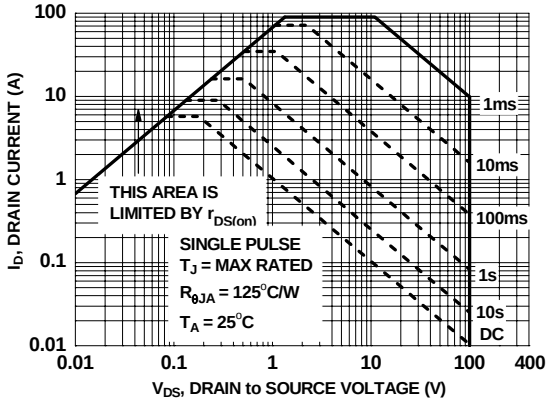



**Figure 11. Forward Bias Safe Operating Area**

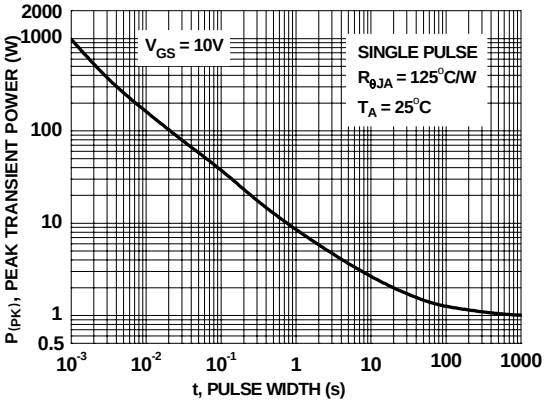



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

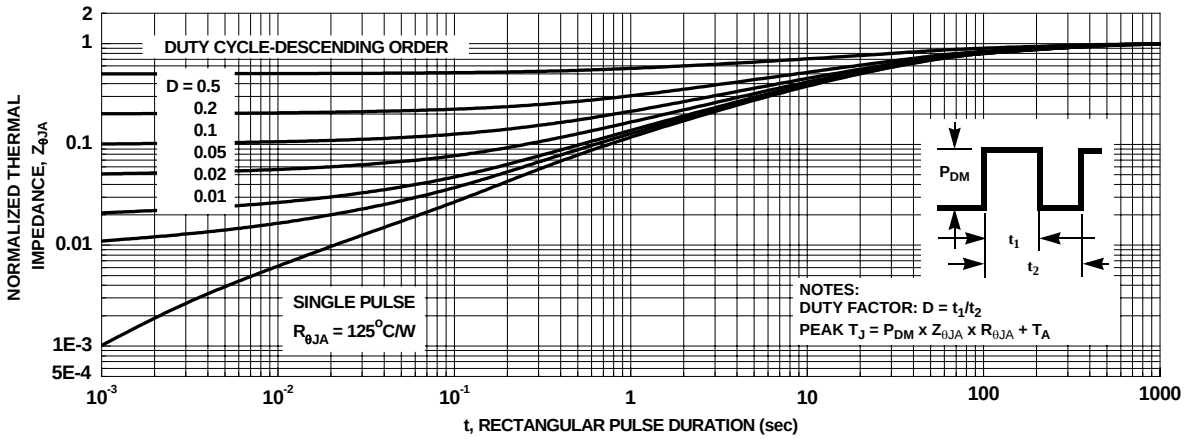
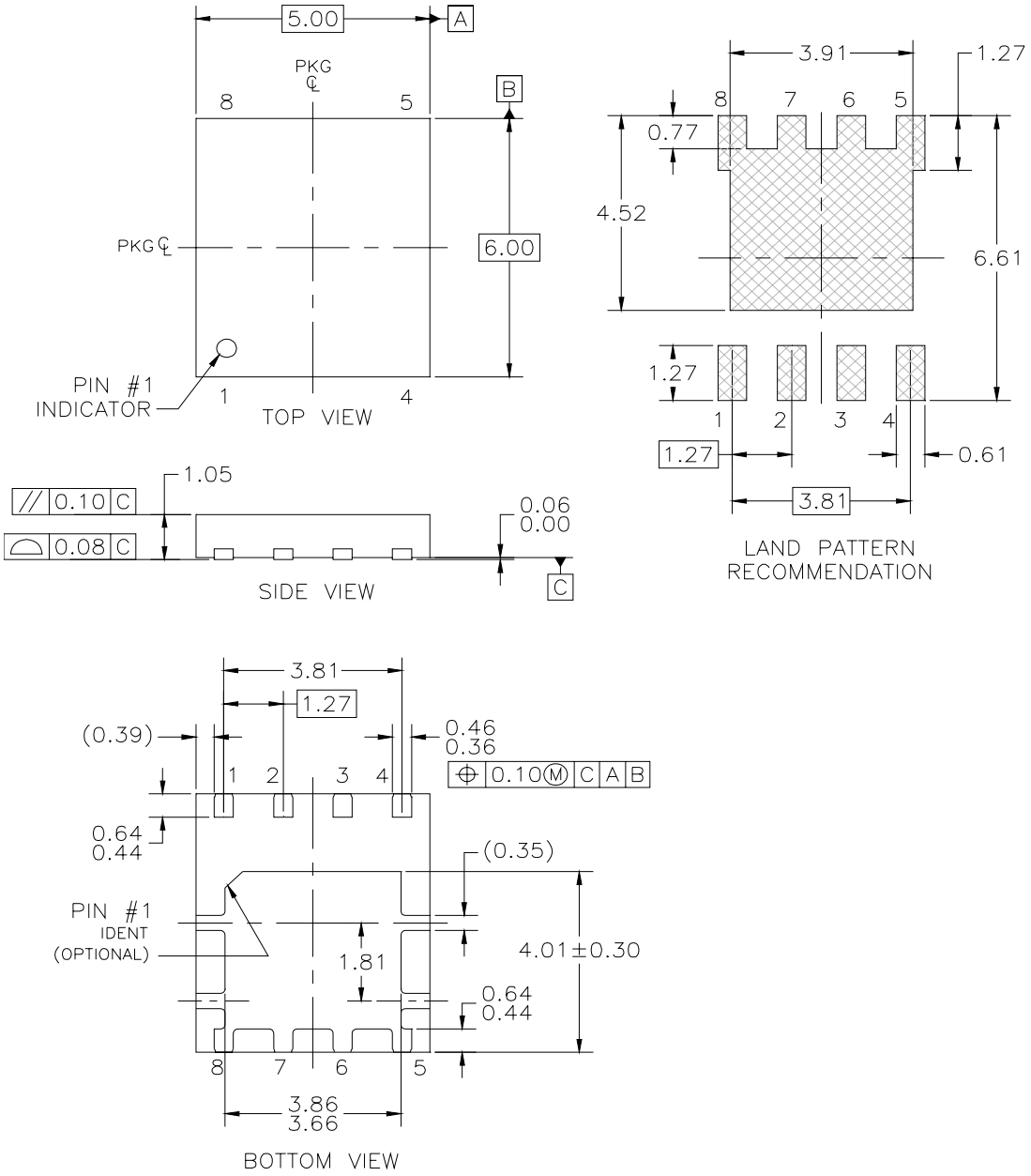



**Figure 13. Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout




NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) NO JEDEC REFERENCE AS OF FEBRUARY 2006

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994

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